R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, on FIGS. 1 and 2 and in the specification as originally filed, for example, on page 5, lines 1-17, on page 8, line 7 through page 9, line 3 and on page 11, lines 1-12. As such, no new matter has been introduced.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-20 under 35 U.S.C. §103(a) as being anticipated by Yamada '537 in view of Aschmann has been obviated by appropriate amendment and should be withdrawn.

Yamada teaches a message passing system for a distributed shared memory multiprocessor system and a message passing method (Title). Aschmann teaches a remote procedure call environment for fault-tolerant heterogeneous, distributed systems (Title).

In contrast, claim 1 of the present invention provides an apparatus comprising a system bus, a shared memory and a multiprocessor logic circuit. The shared memory may be (i) coupled to the system bus and (ii) configured to store data. The multiprocessor logic circuit generally comprises (i) a plurality of processors and (ii) a message circuit. The message circuit is

directly connected to the system bus and configured to pass messages between the plurality of processors. Each of the plurality of processors is directly connected to the system bus and configured to access the shared memory and the message circuit through the system bus. Claims 12 and 13 provide similar limitations. Yamada and Aschmann, alone or in combination, do not appear to teach or suggest a system where (i) the message circuit is directly connected to the system bus and configured to pass messages between the plurality of processors and (ii) each of the plurality of processors is directly connected to the system bus and configured to access the shared memory and the message circuit through the system bus, as presently claimed.

In particular, the processors (elements 19-1, 19-2 and 19-3) do not appear to be directly connected to the so-called system bus (the processor interconnect 25) as presently claimed. Furthermore, the distributed memory shown in FIG. 3 of Yamada (elements 21-1, 21-2 and 21-3) does not appear to be accessible by the processors (elements 19-1, 19-2 and 19-3) through the so-called system bus (the processor interconnect 25) as presently claimed. For example, the processor 19-1 accesses the memory 21-1 through the processor bus 30-1, not the so-called system bus 25 (see FIG. 3 of Yamada and paragraph 4 of the declaration of Kalvin E. Williams). Similarly, the processor 19-2 accesses the memory 21-2 through the processor bus 30-2, not the so-called system bus 25 (see FIG. 3 of Yamada and paragraph 5 of the declaration Kalvin E. Williams). Therefore, Yamada does not disclose or suggest **each** of

the processors accessing the shared memory through a system bus, as presently claimed.

Aschmann does not cure the deficiencies of Yamada. In particular, Aschmann does not appear to teach or suggest a system where (i) the message circuit is directly connected to the system bus and configured to pass messages between the plurality of processors and (ii) each of the plurality of processors is directly connected to the system bus and configured to access the shared memory and the message circuit through the system bus, as presently claimed. Therefore, Yamada and Aschmann do not teach or suggest each and every element of the claimed invention and the rejection should be withdrawn.

Dependent claims 2-11 and 14-20 depend, directly or indirectly, from either claim 1 or claim 13, which are now believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

TELEPHONE INTERVIEW SUMMARY

In a telephone interview on March 31, 2005, between Examiner Courtenay and Applicants' representative, Robert Miller, the independent claims and the Yamada and Aschmann references were discussed. The Examiner identified the specific structures in Yamada which were viewed as reading on the presently claimed elements. Applicants' representative pointed out that assuming, *arguendo*, the structures could be considered similar in type to the

presently claimed elements, the structures were neither arranged nor operated as in the presently claimed invention. Agreement was reached that the amendments to claims 1, 12 and 13 presented herein would distinguish the present invention from the cited references. However, the Examiner stated that further consideration and search would be needed. Agreement was reached that (i) the amendments would be submitted in an RCE, (ii) a new search would be performed and (iii) either a notice of allowance or a non-final Office Action would be issued.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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Dated: April 1, 2005

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Docket No.: 01-213 / 1496.00136